
ARM hardware

reference manual

ARM Evaluation System

Acorn OEM Products



ARM hardware

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Important Information

Wiring the Mains Plug

WARNING: *The ARM Evaluation System must be earthed.*

The wires in the mains lead are coloured in accordance with the following code:

<i>Green and yellow</i>	Earth
<i>Blue</i>	Neutral
<i>Brown</i>	Live

As the colours of the wires may not correspond with the coloured markings identifying the terminals in your plug, proceed as follows:

- The wire which is coloured *green and yellow* must be connected to the terminal in your plug which is marked by the letter E, or by the safety earth symbol or which is identified by being coloured green, or green and yellow.
- The wire which is coloured *blue* must be connected to the terminal which is marked with the letter N, or coloured black.
- The wire which is coloured *brown* must be connected to the terminal which is marked with the letter L, or coloured red.

If the socket outlet available is not suitable for the plug supplied, the plug should be cut off and the appropriate one fitted and wired as previously noted. The moulded plug which was cut off should be disposed of as it would be a potential shock hazard if it were to be plugged in with the cut off end of the mains cord exposed. The moulded plug must be used with the fuse and fuse carrier firmly in place. The fuse carrier is of the same basic colour (though not necessarily the same shade of that colour) as the coloured insert in the base of the plug. Different manufacturers' plugs and fuse carriers are not interchangeable. In the event of loss of the fuse carrier, the moulded plug **MUST NOT** be used. Either replace the moulded plug with another conventional plug (wired as previously described) or obtain a replacement fuse carrier from an authorised Acorn dealer. In the event of the fuse blowing, it should be replaced, after clearing any faults, with a 5 amp fuse that is ASTA approved to BSI 1362.

Exposure

Like all electronic equipment, the ARM Evaluation System should not be exposed to direct sunlight or moisture for long periods.

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1. Introduction

The ARM (Acorn RISC Machine) is a general purpose 32-bit single-chip microprocessor which uses a Reduced Instruction Set Computer architecture in order to achieve high performance.

The Arm contains a 32-bit data bus, 26-bit address bus and a bank of 25 registers, each 32 bits wide.

The instruction set, comprising five basic instruction types, each with an associated 4-bit condition code, is hard wired.

Pipelining is employed, so that all parts of the processing and memory system can be used during every cycle, when executing consecutive register-to-register instructions.

The technology used is 3-micrometres double-level metal CMOS; the chip size is 50 square millimetres, packaged in an 84-pin leadless carrier.

1.1 Features

- 32-bit architecture
- 32-bit data bus
- 26-bit address bus
- 64-MByte uniform address space
- Simple but powerful instruction set
- Good high-level language compiler support
- Support for virtual memory systems
- Fast interrupt response for real-time applications (average interrupt latency less than 2 μ S, worst case less than 6 μ S)
- Average execution rate 3 million instructions per second (MIPS)
- Low power consumption (0.1 W typical)
- Single +5 V supply
- 84-pin JEDEC B leadless chip carrier

1.2 Performance

The ARM microprocessor has been specifically designed for high-performance functions such as real-time artificial intelligence and high-level language applications. The Acorn chip is smaller and the architecture simpler than conventional microprocessors, yet its execution rate of 3 MIPS is one of the fastest available.

The ARM supports virtual memory, has a small optimised instruction set hard wired into a programmable logic array, a heavily pipelined processor, dedicated registers to handle interrupts and a high memory-to-processor bandwidth.

The instructions are all 32 bits wide (one word) and the instruction set consists of five basic types:

- branch (and branch with link)
- data processing
- single data transfer
- block data transfer
- supervisor calls.

The ARM utilises pipelining techniques to gain greater efficiency in the manipulation of instructions. During each processor cycle, one instruction can control the data path while the system decodes a second instruction for the following cycle and fetches a third from memory.

Another performance advantage is the processor's ability to support memory operation in burst (or page) mode. In burst mode, data can be continuously streamed to or from memory, at least twice as fast as in random access mode, depending upon the effect of memory-to-processor interaction.

The ARM performance may be summarised as being:

- approximately 3 MIPS average, using 150 nanoseconds row access DRAMS (evaluation system measured results)
- 8 MIPS peak (first prototype).

This is equivalent to:

- 2 to 4 times DEC VAX 11/780 running high-level benchmarks
- 10 times IBM PC AT running BASIC benchmarks
- A 16.67 MHz Motorola 68020.

(This performance was measured on an ARM Evaluation System.)

The average interrupt latency is less than $2\mu\text{S}$; the maximum latency is less than $6\mu\text{S}$.

2. Standard specifications

2.1 Physical description

The ARM is currently available in an 84-pin JEDEC B ceramic carrier.

A suitable socket, such as AMP, part number 55225-1, may be used for mounting the carrier onto a printed circuit board.

2.2 Power requirements

	absolute maximum rating	nominal
Vcc (supply voltage with respect to Vss)	+6.0 V d.c.*	+5.0 V d.c.
Power dissipation	1 W	

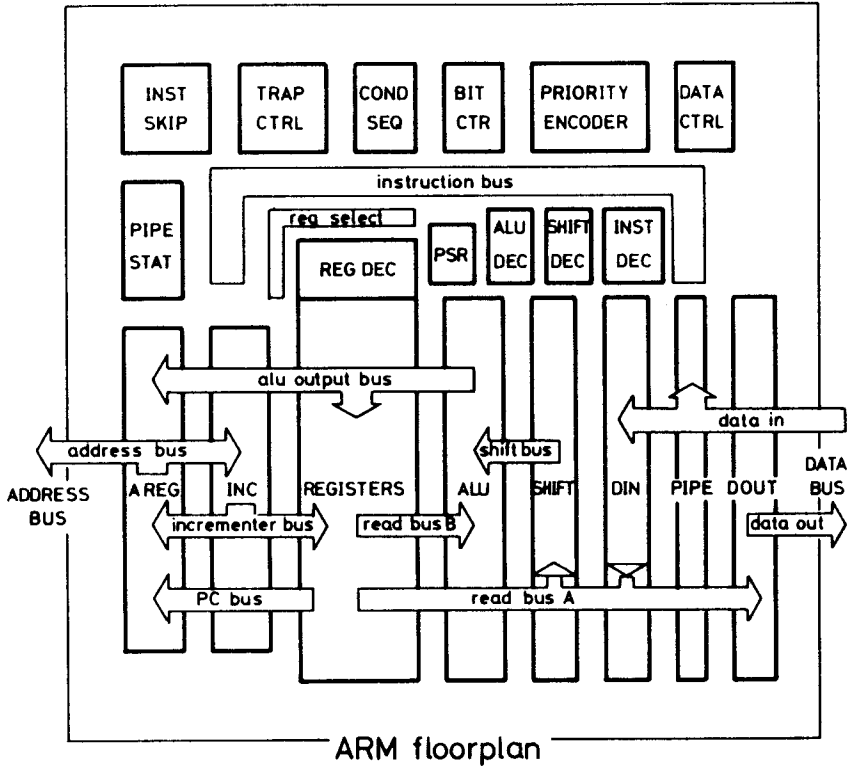
* Note: absolute maximum ratings indicate limits beyond which permanent damage may occur. Operation at these limits is not guaranteed and should be limited to those conditions specified in section 4.1, D.C. characteristics.

2.3 Temperatures

-40 to +70 °C storage without damage.

3. Functional description

3.1 ARM block diagram



3.2 Pin connections, pins 1 to 42

function	name	input/ output	pin number
processor clock	ph2	I	1
processor clock	ph1	I	2
write/not read	rw	O	3
not opcode fetch	opc	O	4
not next cycle memory req.	mreq	O	5
memory abort	abort	I	6
not interrupt request	irq	I	7
not fast interrupt request	fiq	I	8
reset	reset	I	9
not memory translate	trans	O	10
supply voltage	vcc1	I	11
ground	vss1	I	12
not processor mode bit 1	m1	O	13
not processor mode bit 0	m0	O	14
next cycle sequence indicator	seq	O	15
address latch enable	ale	I	16
address line 25	a25	T	17
address line 24	a24	T	18
address line 23	a23	T	19
address line 22	a22	T	20
address line 21	a21	T	21
address line 20	a20	T	22
address line 19	a19	T	23
address line 18	a18	T	24
address line 17	a17	T	25
address line 16	a16	T	26
address line 15	a15	T	27
address line 14	a14	T	28
address line 13	a13	T	29
address line 12	a12	T	30
address line 11	a11	T	31
supply voltage	vcc2	I	32
ground	vss2	I	33

function	name	input/ output	pin number
address line 10	a10	T	34
address line 9	a9	T	35
address line 8	a8	T	36
address line 7	a7	T	37
address line 6	a6	T	38
address line 5	a5	T	39
address line 4	a4	T	40
address line 3	a3	T	41
address line 2	a2	T	42
address line 1	a1	T	43
address line 0	a0	T	44
address bus Tri-state enable	abe	I	45
data line 0	d0	B	46
data line 1	d1	B	47
data line 2	d2	B	48
data line 3	d3	B	49
data line 4	d4	B	50
data line 5	d5	B	51
data line 6	d6	B	52
data line 7	d7	B	53
ground	vss3	I	54
supply voltage	vcc3	I	55
data line 8	d8	B	56
data line 9	d9	B	57
data line 10	d10	B	58
data line 11	d11	B	59
data line 12	d12	B	60
data line 13	d13	B	61
data line 14	d14	B	62
data line 15	d15	B	63
data line 16	d16	B	64
data line 17	d17	B	65
data line 18	d18	B	66
data line 19	d19	B	67
data line 20	d20	B	68

function	name	input/ output	pin number
data line 21	d21	B	69
data line 22	d22	B	70
data line 23	d23	B	71
data line 24	d24	B	72
data line 25	d25	B	73
data line 26	d26	B	74
ground	vss4	I	75
supply voltage	vcc4	I	76
data line 27	d27	B	77
data line 28	d28	B	78
data line 29	d29	B	79
data line 30	d30	B	80
data line 31	d31	B	81
not connected	-	-	82
data bus enable	dbe	I	83
word/not byte transfer	bw	O	84

symbols:

I = input to chip

O = output from chip

B = bi-directional

T = tri-state output.

3.3 ARM element functions

Referring to the block diagram in section 3.1, the functions of the main units are as follows:

element	function
alu	arithmetic logic unit
registers	a bank of 25 32-bit registers
shift	a 32-bit barrel shifter to assist arithmetic and logical register operations with a rotate capability

element	function
data in/out	32-bit data bus
din	the data input control logic, which extracts the required field from the incoming data or instruction
dout	the data output control block, which replicates a byte across the data bus for byte write operations
addbus	26-bit address bus
inc	the address incrementer
areg	the current address register
pipe	the instruction pipeline
inst skip	controls the skipping (non-execution) of instructions which do not meet the required condition codes
trap cntl	handles the synchronisation and prioritisation of interrupts, exceptions, aborts and reset
cond seq	evaluates the instruction condition field and controls the instruction cycle sequence
bit ctr	counts the number of 1s in the 16-bit field used by load and store multiple instructions
priority encoder	finds the least significant 1 in the 16-bit field used by load and store multiple operations
data ctrl	controls the flow of data into the processor
pipe stat	keeps the status of instructions in the pipeline, differentiating between valid instructions and those which cause an abort

element	function
instruction bus	carries the current instruction for decoding by the various control blocks
reg select	selects the fields in the current instruction which define the registers to be used
reg dec	decodes the selected fields to access particular registers
psr	the program status register, which contains the ALU flags, the interrupt masks and the processor mode bits
alu dec	a PLA (programmable logic array) which controls the function of the ALU
shift dec	the barrel shifter control
inst dec	a PLA which performs the top-level instruction decoding.

3.4 ARM operational description

The ARM is a 32-bit single chip microprocessor based on a reduced instruction set architecture.

The chip runs on a non-overlapping two-phase clock and all data path operations take place in one clock cycle (which is clock phase 1 plus clock phase 2).

The heart of the chip is the register bank, which contains 25 32-bit registers of which 16 are visible to the programmer. The remainder of these registers are used to support the supervisor, the interrupt and the fast interrupt modes. The register bank contains two read buses and one write bus. The two read buses enable both ALU operands to be fetched from the register bank simultaneously:

- one operand is passed through the barrel shifter before going into the ALU (the fetches taking place during clock phase 1). The result may be written back to a register during clock phase 2
- the second (shifted) operand may be obtained from an immediate field in the instruction, rather than from a register.

The memory address is held in the address register and, associated with this register, there is a dedicated address incremter. The address for the next memory cycle may come from the ALU or be forced to an exception value, but, under normal operation, it is taken from the incremter. When the incremter is the address source, this fact is indicated by asserting the SEQ pin. External memory control can then predict the next address and take decisions as to whether address translation is necessary or DRAM page mode can be used.

Note: using DRAM page mode enables the cycle to proceed at double speed (or greater) and saves power compared to a full RAM access. When executing typical program code, page mode accesses are used for 70% to 90% of all memory cycles.

The instruction pipeline holds instructions awaiting execution. It is synchronous, fetches instructions at defined times, and is of minimum length to keep all sections of the processor busy during consecutive register to register instructions. As one such instruction is being executed on the data path, the next is being decoded while a third is being fetched from memory. Each instruction occupies a part of the processor for three cycles, but the pipelining technique used allows the execution of one instruction per cycle.

Output word data is sent as 32-bit words, aligned on the data bus. Byte data is replicated four times across the data bus and the correct memory byte can be written by activating only the relevant column address strobe (CAS). The *bw* (word/not byte) signal indicates a byte transfer and *a0* & *a1* (address lines) indicate the byte within the word.

Input word-aligned data is transferred to the target register. Input bytes are field extracted, zero extended in the data input block (*din*) and rotated into the lowest byte position by the barrel shifter, before being placed in the target register.

The priority encoder is used only in block transfer instructions. These allow any defined register subset to be transferred into successive memory words during consecutive cycles using sequential memory modes. Register saving on subroutine entry therefore exploits the most efficient memory transfer mode and this can include stacking the return address from the link register. Restoring registers and returning may be performed by load multiple, loading the return address directly into the processor rather than via the link register.

the ARM supports eight exceptions, five caused by external hardware, three by internal hardware

External hardware exceptions:

- (1) the asynchronous reset signal clears the current instruction and forces execution from location 0
- (2) interrupt (*irq*) is synchronised and, when enabled, forces the processor to begin execution at a fixed memory location on completion of the current instruction
- (3) fast interrupt (*fiq*), as described in (2) above, *irq*
- (4) two (abort) exceptions which modify the consequences of the current instruction to ensure that a restart will be possible before forcing the execution address the forced address depends on whether the abort was the result of a data transfer or instruction fetch.

Internal hardware exceptions:

- (1) supervisor calls are forced to a fixed memory location and enter supervisor mode. This is a protected state and may only be entered from user mode via an exception, allowing trusted software to take control in a system with protected memory
- (2) Undefined instructions are identical to supervisor calls except that they use a different exception location. They are (by convention) reserved for future expansion and the trap may be used for the emulation of future additions to the instruction set
- (3) the address exception trap, caused by attempts to access data outside the 64-Mbyte addressable range.

The interrupt priorities are:

- reset (highest)
- address exception
- data abort
- fiq
- irq
- prefetch abort
- undefined instruction
- software interrupt (lowest)

Note: not all exceptions can occur at once. Address exception and Data abort are mutually exclusive, as are Undefined instruction and Software interrupt. A summary list and a description of the instruction set is given in appendix A.

4. Signal description

4.1 D.C. characteristics

name	min	typical	max	unit	conditions
Vil	-0.30		+0.80	V	except clock
Vih	+2.40		Vcc +0.30	V	except clock
Vcil	-0.30		+0.30	V	clock
Vcih	Vcc -0.30		Vcc +0.30	V	clock
Vol			+0.50	V	Iol = -3.60 mA
Voh	Vcc -0.50			V	Ioh = +3.00 mA
Vcc	+4.75	+5.00	+5.25	V	
Icc		20.00		mA	measured at Vcc = 5.00 V

symbols

Vil	signal input low voltage
Vih	signal input high voltage
Vcil	clock input low voltage
Vcih	clock input high voltage
Vol	signal output low voltage
Voh	signal output high voltage
Iol	signal output low current
Ioh	signal output high current
Vcc	supply voltage
Vss	ground reference
Icc	supply current